CLAIMS

What we claim is:

1. Emulated EEPROM memory device of the type included into a memory macrocell (1) which is embedded into an integrated circuit comprising also a microcontroller and including a Flash EEPROM memory structure formed by a predetermined number of sectors (F0, F1, F2, F3, F4, F5), characterized in that at least two sectors (E0, E1) of the Flash memory structure are used to emulate EEPROM byte alterability.

2. Emulated EEPROM memory device according to claim 1, characterized in that said EEPROM byte alterability is emulated by hardware means.

3. Emulated EEPROM memory device according to claim 1, characterized in that 8 Kbyte of the Flash memory portion are used to emulate 1 kbyte of an EEPROM memory portion.

4. Emulated EEPROM memory device according to claim 1, characterized in that first and second EEPROM emulated sectors (E0, E1) are each divided in a pre-determined number of blocks (BLOCK 0, ..., BLOCK3) of the same size and each block is divided in pages.

5. Emulated EEPROM memory device according to claim 1, characterized in that a state machine (15) is provided for controlling an address counter (20) which is output connected to an internal address bus (21) running inside the memory macrocell (1), said address counter (20) receiving control signals from the state machine (15) in order to control the loading of hard-coded addresses in volatile or non-volatile registers (25) which are read and

updated by the microcontroller during a reset phase or by the state machine (15) after an EEPROM update.

6. Emulated EEPROM memory device according to claim 5, characterized in that said address bus (21) is connected to the input of a RAM buffer (22) which is used for the page updating of the EEPROM including two additional byte (23, 24) for storing the page address during a page updating phase.

7. Emulated EEPROM memory device according to claim 1, characterized in that Flash and EEPROM memories operations are controlled through a register interface (7) mapped into the memory (1).

8. Method for emulating the features of a EEPROM memory device incorporated into a memory macrocell (1) which is embedded into an integrated circuit comprising also a microcontroller and including a Flash EEPROM memory structure formed by a predetermined number of sectors (F0, F1, F2, F3, F4, F5), characterized in that at least two sectors (E0, E1) of the Flash memory structure are used to emulate EEPROM byte alterability by dividing each of said two sector in a pre-determined number of blocks (BLOCK 0, ..., BLOCK3) of the same size and each block in a pre-determined number of pages and updating the emulated EEPROM memory portion programming different memory locations in a single bit mode.

9. Method according to claim 8, characterized in that at each page update selected page data are moved to the next free block and, when an EEPROM sector is full, all the pages are swapped to the other EEPROM sector.

10. Integrated microcontroller having an on-board non-

volatile Flash EEPROM memory portion structure formed by a predetermined number of sectors, characterized in that at least two sectors of the Flash memory structure are used to emulate EEPROM byte alterability.